MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR FIELD PROGRAMMABLE LOGIC ARRAY (FPLA) 16 X 48 X 8, MONOLITHIC SILICON

This specification is approved for use by Rome Air Development Center, Department of the Air Force, and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, bipolar, field programmable logic array (FPLA) microcircuits which employ thin film nichrome resistors (NICr) as the fusible link or programming element. Three product assurance classes and a choice of case outline/lead material and finish are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device types shall be as follows:

Device type	Circuit
01	16 X 48 X 8 logic array with uncommitted collector
02	16 X 48 X 8 logic array with active pull-up and a third high-impedance state output.

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline (see MIL-M-38510, appendix C)
X	(28-lead .605 X 1.405, dual-in-line pack)

1.3 Absolute maximum ratings.

Supply voltage	-0.5 to 7.0 Vdc
Input voltage range	0.5 Vdc at -10 mA to 5.5 Vdc
Storage temperature range	-65° to +150°C
Lead temperature (soldering, 10 seconds)	260°C
Thermal resistance, junction to case 1/	θ_{JC} = 27°C/W
Output voltage applied	-0.4 to +5.5 Vdc
Output sink current	9.6 mA
Maximum power dissipation, P_D 2/	2.0 W
Maximum junction temperature	T_J = 175°C

1.4 Recommended operating conditions.

Supply voltage	4.5 Vdc minimum to 5.5 Vdc maximum
Minimum high-level input voltage	2.0 Vdc
Maximum low-level input voltage	0.8 Vdc
Case operating temperature range	-55° to 125°C

1/ Heat sinking is recommended to reduce the junction temperature.
2/ Shall withstand the added P_D due to short-circuit condition (e.g., I_{OS}) test.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

2. APPLICABLE DOCUMENTS

2.1 Issues of documents. The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer-programmed devices are delivered to the user, an altered item drawing shall be prepared by the procuring activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test as per table VII (a minimum of 50 percent of the total number of gates programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. Case outlines shall be in accordance with MIL-M-38510 and 1.2.3 herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements shall be as specified in table III and (where applicable), the altered item drawing for the applicable device type and device class. The subgroups of table III which constitute the minimum electrical test requirements for screening, qualifications, and quality conformance by device class are specified in table II.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/	Device types	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	V_{CC} = 4.5 V; I_{OH} = -2 mA	02	2.4		V
Low-level output voltage	V_{OL}	V_{CC} = 5.5 V; I_{OL} = 9.6 mA	01,02		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V; I_{IN} = -18 mA	01,02		-1.2	V
Maximum collector cut-off current	I_{CEX}	V_{CC} = 5.5 V; V_O = 5.5 V	01		100	µA
High-impedance (off-state) output high current	I_{OHZ}	V_{CC} = 5.5 V; V_O = 5.5 V	02		100	µA
High-impedance (off-state) output low current	I_{OLZ}	V_{CC} = 5.5 V; V_O = 0.45 V	02		-60	µA
High-level input current	I_{IH}	V_{CC} = 5.5 V; V_{IN} = 5.5 V	01,02		50	µA
Low-level input current	I_{IL}	V_{CC} = 5.5 V; V_{IN} = 0.45 V	01,02	-1	-250	µA
Short circuit output current	I_{OS} 2/	V_{CC} = 5.5 V; V_{OUT} = GND	02	-10	-85	mA
Supply current	I_{CC}	V_{CC} = 5.5 V; V_{IN} = 0; outputs = open	01,02		180	mA
Propagation delay time high-to-low level logic, input to output	t_{PHL1} (t_{IA})	V_{CC} = 4.5 V and 5.5 V; C_L = 30 pF (See figure 5)	01,02		80	ns
Propagation delay time Low-to-high level logic, input to output	t_{PLH1} (t_{IA})		01,02		80	ns
Propagation delay time high-to-low level logic, enable to output	t_{PHL2} (t_{EC})		01,02		50	ns
Propagation delay time low-to-high level logic, enable to output	t_{PLH2} (t_{CO})		01,02		50	ns

1/ Complete terminal conditions shall be specified in table III.

2/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.7 Processing options. Since the FPLA is an unprogrammed device capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.7.1 Unprogrammed FPLA delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1, tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed FPLA delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)		
	Class S devices	Class B devices	Class C devices
Interim electrical parameters (pre burn-in) (method 5004)	1	1	None
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*,8	1*,2,3,7*,8	1
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8, 9,10,11	1*,2,3,7*,8, 9	1,7,9
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11
Group C end-point electrical parameters (method 5005)	N/A	1,2,3,7,8	1,2,3,7
Group D end-point electrical parameters (method 5005)	1,2,3,7,8	1,2,3,7,8	1,2,3,7

1/ (*) indicates PDA applies to subgroups 1 and 7 (see 4.2c).

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroup 7 and 8 shall consist of verifying the pattern specified.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

Device types 01 and 02

Case X

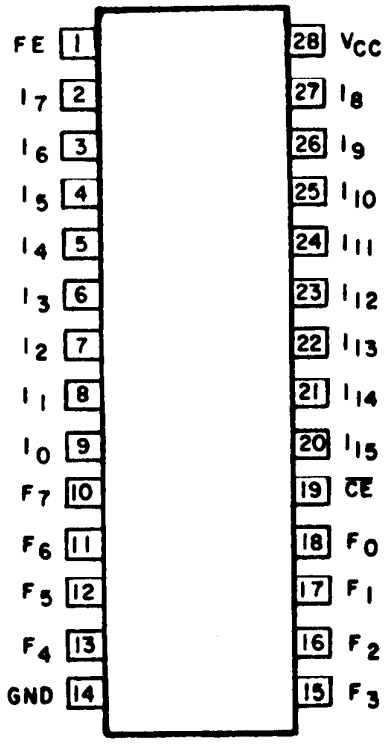


FIGURE 1. Terminal connections.

Circuit type	$\overline{CE}$	Address																Output level								Device type
		I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0	
A	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	01,02
B	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	01,02
A,B	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1/	1/	1/	1/	1/	1/	1/	1/	01
A,B	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	02

NOTES:
1. Output disabled.
2. X = Input may be high, low level, open circuit or as defined in Appendix.
3. L = Low
4. H = High
5. Hi Z = High impedance.

FIGURE 2. Truth table (unprogrammed).

Device types 01 and 02

Circuit A

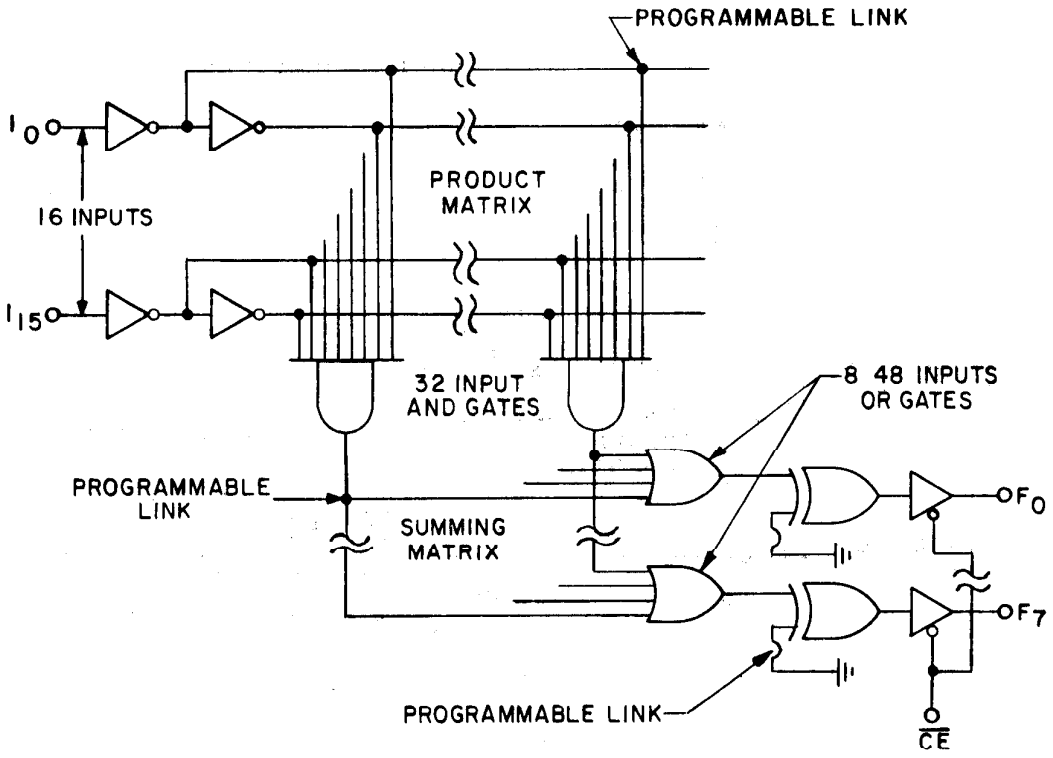


FIGURE 3. Logic diagram.

Device types 01 and 02

Circuit B

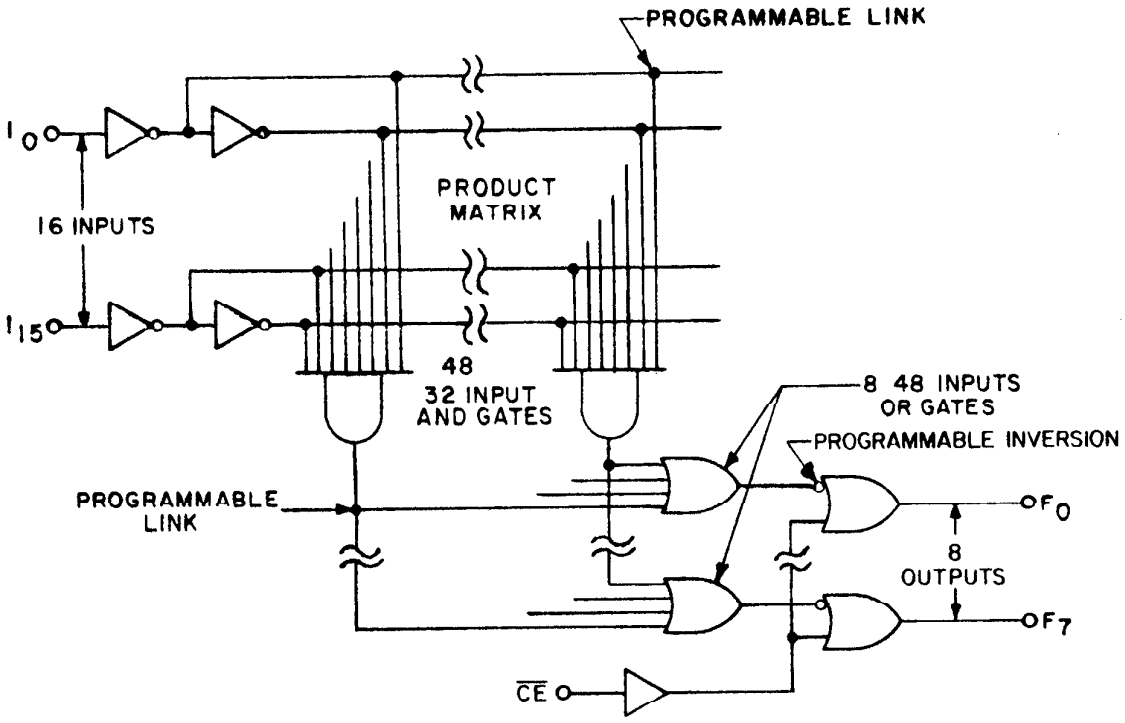
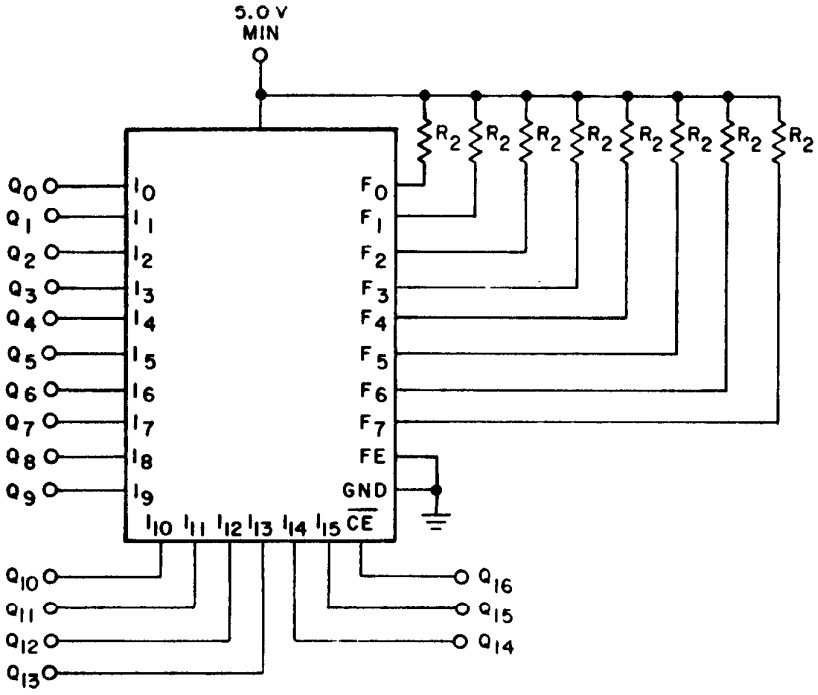


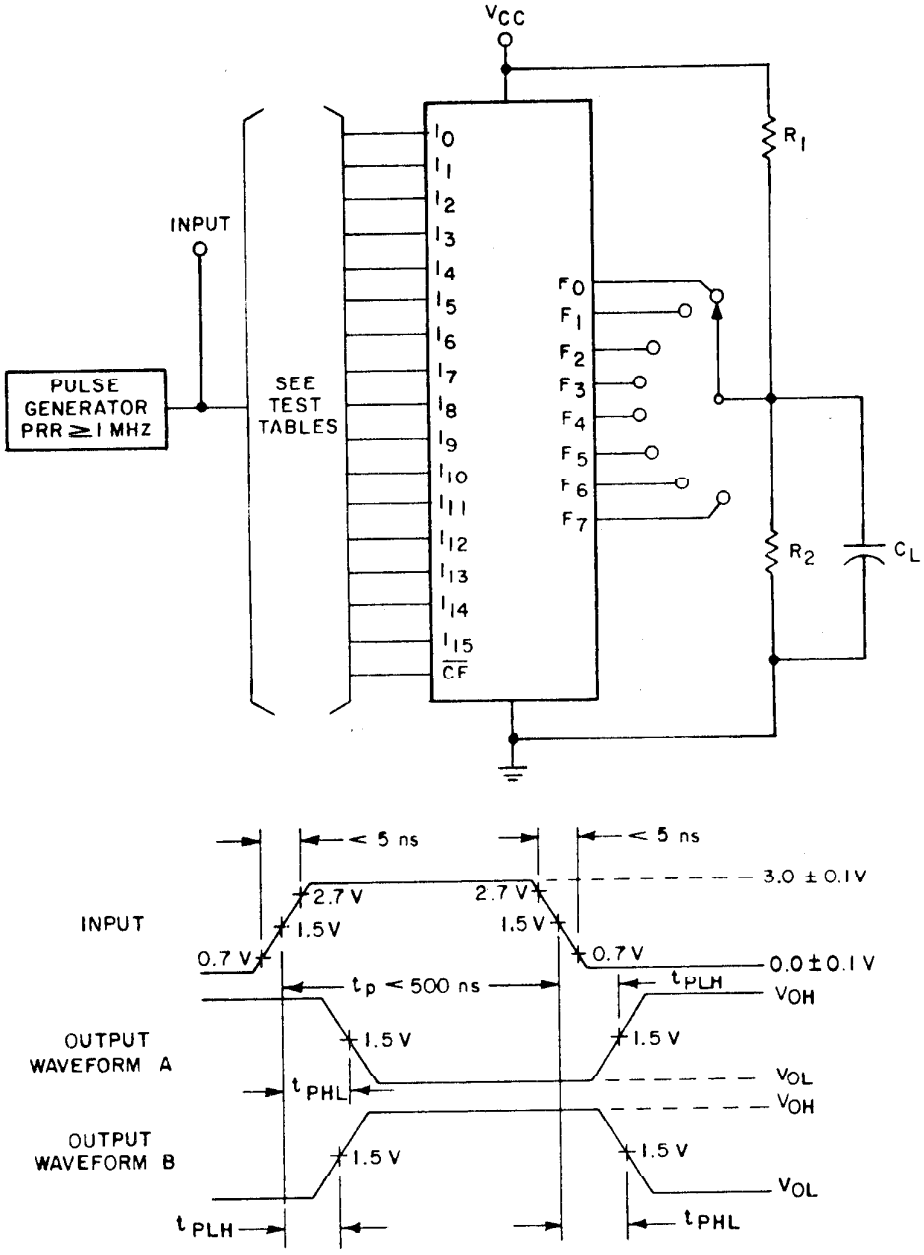
FIGURE 3. Logic diagram - Continued.



NOTES:
1. R2 = 330Ω ±5%. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics: V_{IL} = -0.5 V minimum to 0.8 V maximum; V_{IH} = 2.0 V minimum to 5.5 V maximum; 50% ±15% duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V minimum at the device V_{CC} terminal.
4. Input frequencies are as follows:

Input	Frequency (±50%)
Q_0	f_0 = 100 kHz Min
Q_1	f_1 = 1/2 f_0
Q_2	f_2 = 1/2 f_1
Q_3	f_3 = 1/2 f_2
Q_4	f_4 = 1/2 f_3
Q_5	f_5 = 1/2 f_4
Q_6	f_6 = 1/2 f_5
Q_7	f_7 = 1/2 f_6
Q_8	f_8 = 1/2 f_7
Q_9	f_9 = 1/2 f_8
Q_{10}	f_{10} = 1/2 f_9
Q_{11}	f_{11} = 1/2 f_{10}
Q_{12}	f_{12} = 1/2 f_{11}
Q_{13}	f_{13} = 1/2 f_{12}
Q_{14}	f_{14} = 1/2 f_{13}
Q_{15}	f_{15} = 1/2 f_{14}
Q_{16}	f_{16} = 1/2 f_{15}

FIGURE 4. Burn-in and life test circuit.



NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting FPLA.
2. C_L = 30 pF minimum, including jig and probe capacitance; R_1 = 300Ω ±25% and R_2 = 600Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 5. Switching time test circuit.

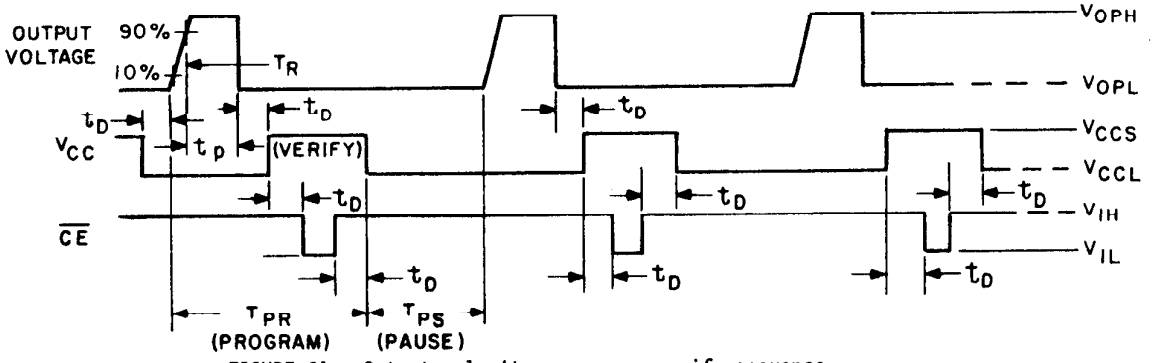


FIGURE 6A. Output polarity program - verify sequence.

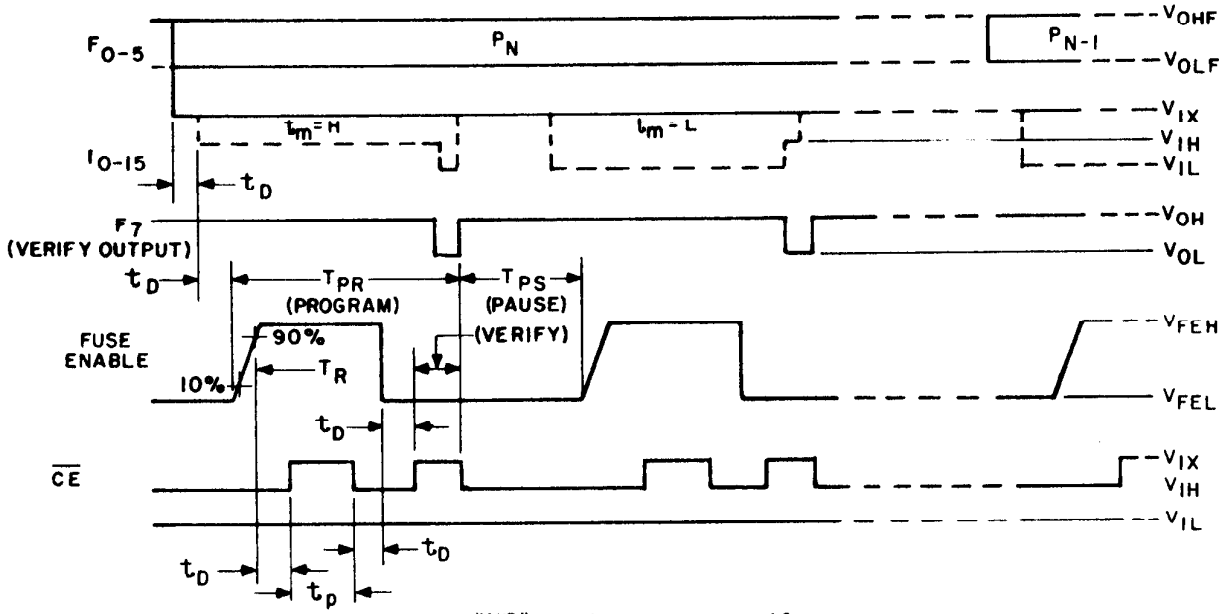


FIGURE 6B. "AND" matrix program - verify sequence.

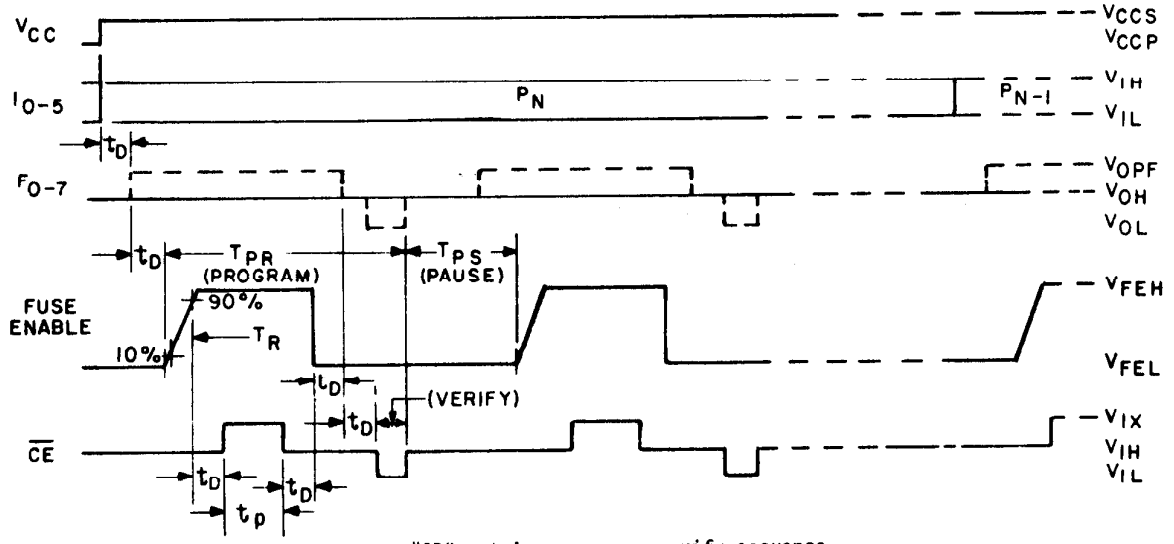
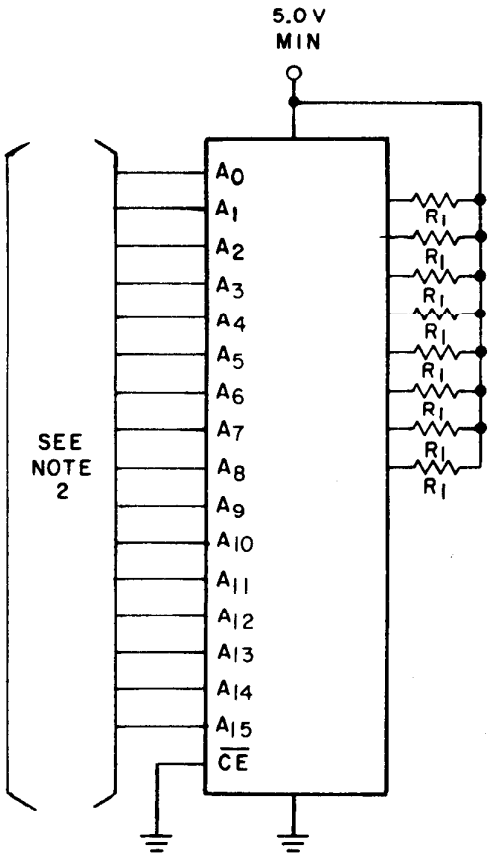


FIGURE 6C. "OR" matrix program - verify sequence.

FIGURE 6. Typical program - verify sequence circuit A.



NOTES:
1. R_1 = 4.7 kΩ ±5%. All outputs shall have separate identical loads.
2. For the freeze-out test, all address inputs shall be either high, low, or open.
3. Burn-in circuit may be used to perform this test. (See 4.3 d.) All address input shall be either high, low, or open.

FIGURE 7. Freeze-out test bias configuration.

TABLE II. Group A inspection for device type 01.

Subgroup	Symbol	MIL-STD-883 method	Case X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits		Unit
			Test No.	FE	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	GND	F_3	F_2	F_1	F_0	CE	I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	V_{CC}		Min	Max	
1 T_C = 25°C	V_{IC}		1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17		-18 mA	-11 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA					GND					-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	4.5 V	I_C I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 I_8 I_9 I_{10} I_{11} I_{12} I_{13} I_{14} I_{15} CE		-1.2	V
	V_{OL}	3007	18 19 20 21 22 23 24 25		4/	4/	4/	4/	4/	4/	4/	4/	9.6 mA	9.6 mA	9.6 mA	9.6 mA		9.6 mA	9.6 mA	9.6 mA	9.6 mA		4/	4/	4/	4/	4/	4/	4/	4/	5.5 V	F_7 F_6 F_5 F_4 F_3 F_2 F_1 F_0		0.5	V
	I_{IL}	3009	26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42		0.45 V	0.45 V	0.45 V	0.45 V	0.45 V	0.45 V	0.45 V	0.45 V										0.45 V	0.45 V	0.45 V	0.45 V	0.45 V	0.45 V	0.45 V	0.45 V		I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0 F_7 F_6 F_5 F_4 F_3 F_2 F_1 F_0 CE	-1	-250	µA
	I_{IH}	3010	43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59		5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V										5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0 F_7 F_6 F_5 F_4 F_3 F_2 F_1 F_0 CE		50	µA

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case X Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits Min	Test limits Max	Unit
				FE	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	GND	F_3	F_2	F_1	F_0	$\overline{CE}$	I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	V_{CC}				
1 T_C = 25°C	I_{CEX}		60 61 62 63 64 65 66 67										5.5 V	5.5 V	5.5 V	5.5 V	GND	5.5 V	5.5 V	5.5 V	5.5 V	4.5 V									5.5 V	I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7		100	µA
	I_{CC}	3005	68		GND	GND	GND	GND	GND	GND	GND	GND										GND	GND	GND	GND	GND	GND	GND	GND		I_{CC}		180	mA
2	Same tests and terminal conditions as in subgroup 1, except T_C = 125°C.																																		
3	Same tests and terminal conditions as in subgroup 1, except T_C = -55°C.																																		
7 T_C = 25°C	Functional test		69		1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	GND	1/	1/	1/	1/	GND	1/	1/	1/	1/	1/	1/	1/	1/	1/	(8) Outputs		1/	
8	Same tests and terminal conditions as in subgroup 7, except T_C = -55°C.																																		
9 T_C = 25°C	t_{PHL1}	3003 Fig. 5	70		2/	2/	2/	2/	2/	2/	2/	2/	3/	3/	3/	3/	GND	3/	3/	3/	3/	GND	2/	2/	2/	2/	2/	2/	2/	2/	2/	(8) Outputs		80	ns
	t_{PLH1}		71																														80	
	t_{PHL2}		72																														50	
	t_{PLH2}		73																														50	
10	Same tests, terminal conditions and limits as subgroup 9, except T_C = 125°C.																																		
11	Same tests, terminal conditions and limits as subgroup 9, except T_C = -55°C.																																		

1/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II). The functional tests shall be accomplished as defined in the appendix for unprogrammed devices.

2/ (Programmed device) The test will check all inputs, gates, and outputs that have been programmed. Propagation tests for t_{PHL1}, t_{PLH1}, t_{PHL2}, t_{PLH2} is also measured. This test shall be performed with V_{CC} = 4.5 V, and V_{CC} = 5.5 V.

3/ The outputs are loaded per figure 5.

4/ For programmed devices, select an appropriate set of inputs to acquire the desired output state.

TABLE II. Group A inspection for device type 02.

Subgroup	Symbol	MIL-STD-883 method	Case X / Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits Min	Test limits Max	Unit
				FE	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	GND	F_3	F_1	F_1	F_0	CE	I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	V_{CC}				
1 T_C = 25°C	V_{IC}		1		-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA	-18 mA					GND														4.5 V	I_0		-1.2	V
			2			-18 mA																									I_1			
			3				-18 mA																									I_2			
			4					-18 mA																								I_3			
			5						-18 mA																							I_4			
			6							-18 mA																						I_5			
			7								-18 mA																					I_6			
			8									-18 mA																				I_7			
			9																													I_8			
			10																													I_9			
			11																													I_{10}			
			12																													I_{11}			
			13																													I_{12}			
			14																													I_{13}			
			15																													I_{14}			
			16																													I_{15}			
			17																													CE			
	V_{OL}	3007	18		4/	4/	4/	4/	4/	4/	4/	4/						9.6 mA	9.6 mA	9.6 mA	9.6 mA	9.6 mA	4/	4/	4/	4/	4/	4/	4/	4/	5.5 V	F_0		0.5	
			19																													F_1			
			20																													F_2			
			21																													F_3			
			22																													F_4			
			23																													F_5			
			24																													F_6			
			25																													F_7			
	V_{OH}	3006	26															-2 mA	-2 mA	-2 mA	-2 mA	-2 mA									4.5 V	F_0	2.4		
			27																													F_1			
			28																													F_2			
			29																													F_3			
			30																													F_4			
			31																													F_5			
			32																													F_6			
			33																													F_7			
	I_{IL}	3009	34																												5.5 V	I_0	-1	-250	μA
			35																													I_1			
			36																													I_2			
			37																													I_3			
			38																													I_4			
			39																													I_5			
			40		0.45 V																											I_6			
			41			0.45 V																										I_7			
			42				0.45 V																									I_8			
			43					0.45 V																								I_9			
			44						0.45 V																							I_{10}			
			45							0.45 V																						I_{11}			
			46								0.45 V																					I_{12}			
			47									0.45 V																				I_{13}			
			48																				0.45 V									I_{14}			
			49																					0.45 V								I_{15}			
			50																			0.45 V										CE			
	I_{IH}	3010	51																													I_0		50	
			52																													I_1			
			53																													I_2			
			54																													I_3			
			55																													I_4			
			56																													I_5			
			57																													I_6			
			58		5.5 V																											I_7			
			59			5.5 V																										I_8			
			60				5.5 V																									I_9			
			61					5.5 V																								I_{10}			
			62						5.5 V																							I_{11}			
			63							5.5 V																						I_{12}			
			64								5.5 V																					I_{13}			
			65									5.5 V																				I_{14}			
			66																													I_{15}			
			67																													CE			

See footnotes at end of table.

TABLE III. Group A inspection for device type 02 - Continued.

Subgroup	Symbol	MIL-STD-883 method	Case X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	Measured terminal	Test limits Min	Test limits Max	Unit
			Test No.	FE	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	GND	F_3	F_2	F_1	F_0	$\overline{CE}$	I_{15}	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	V_{CC}				
1 T_C = 25°C	I_{OHZ}		68	4/	4/	4/	4/	4/	4/	4/	4/	4/					GND			5.5 V	5.5 V	GND	4/	4/	4/	4/	4/	4/	4/	4/	5.5 V	O_0		100	µA
			69															5.5 V													O_1			
			70													5.5 V			5.5 V													O_2			
			71												5.5 V																	O_3			
			72											5.5 V																		O_4			
			73										5.5 V																			O_5			
			74																													O_6			
			75																													O_7			
	I_{OLZ}		76																		0.45 V											O_0	-60		
			77																	0.45 V												O_1			
			78																0.45 V													O_2			
			75															0.45 V														O_3			
			80																													O_4			
			81												0.45																	O_5			
			82											0.45																		O_6			
			83										0.45																			O_7			
	I_{OS}	3011	84																		GND											O_0	-10	-85	mA
			85																	GND												O_1			
			86																GND													O_2			
			87															GND														O_3			
			88																													O_4			
			89												GND																	O_5			
			90											GND																		O_6			
			91										GND																			O_7			
	I_{CC}	3005	92		GND	GND	GND	GND	GND	GND	GND	GND										GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{CC}		180	mA
2	Same tests and terminal conditions as in subgroup 1, except T_C = 125°C.																																		
3	Same tests and terminal conditions as in subgroup 1, except T_C = -55°C.																																		
7 T_C = 25°C	Functional test	1/	93		1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	GND	1/	1/	1/	1/	GND	1/	1/	1/	1/	1/	1/	1/	1/	1/	8) Outputs			
8	Same tests and terminal conditions as in subgroup 7, except T_C = 125°C and T_C = -55°C.																																		
9 T_C = 25°C	t_{PHL1}	3003 Fig. 5	94		2/	2/	2/	2/	2/	2/	2/	2/	3/	3/	3/	3/	GND	3/	3/	3/	3/	GND	2/	2/	2/	2/	2/	2/	2/	2/	2/	8) Outputs		80	ns
	t_{PLH1}		95																															80	
	t_{PHL2}		96																															50	
	t_{PLH2}		97																															50	
10	Same tests, terminal conditions and limits as subgroup 9, except T_C = 125°C.																																		
11	Same tests, terminal conditions and limits as subgroup 9, except T_C = -55°C.																																		

1/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II). The functional tests shall be accomplished as defined in the appendix for unprogrammed devices.

2/ (Programmed device) The test will check all inputs, gates, and outputs that have been programmed. Propagation test for t_{PHL1}, t_{PLH1}, t_{PHL2}, t_{PLH2} is also measured. This test shall be performed with V_{CC} = 4.5 V, and V_{CC} = 5.5 V.

3/ The outputs are loaded per figure 5.

4/ For programmed devices, select an appropriate set of inputs to acquire the desired output state.

TABLE IV. Programming characteristics - Circuit A. 4/

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Type	Max	
V_{CCS} 1/2/	V_{CC} supply (program/verify "OR" verify output program)	I_{CCS} = 550 mA, min (Transient or steady state)	8.25	8.5	8.75	V
V_{CCL}	V_{CC} supply (Program output polarity)		0	0.4	0.8	V
I_{CCS}	I_{CC} limit (Program "OR")	V_{CCS} = +8.50 ±.25 V	550		1,000	mA
V_{OPH} 2/	Output voltage (Program output polarity)	I_{OPH} = 300 ±25 mA	16.0	17.0	18.0	V
V_{OP1}	Output voltage (Idle)		0	0.4	0.8	V
I_{OPH}	Output current limit (Program output polarity)	V_{OPH} = +17 ±1.0 V	275	300	325	mA
V_{IH}	Input voltage (Logic "1")		2.4		5.5	V
V_{IL}	Input voltage (Logic "0")		0	0.4	0.8	V
I_{IH}	Input current (Logic "1")	V_{IH} = +5.5 V			50	µA
I_{IL}	Input current (Logic "0")	V_{IL} = 0 V			-500	µA
V_{OHF}	Forced output (Logic "1")		2.4		5.5	V
V_{OLF}	Forced output (Logic "0")		0	0.4	0.8	V
I_{OHF}	Output current (Logic "1")	V_{OHF} = +5.5 V			100	µA
I_{OLF}	Output current (Logic "0")	V_{OLF} = 0 V			-1	mA
V_{IX}	CE program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10 V			2.5	mA
I_{IX2}	CE input current	V_{IX} = +10 V			5.0	mA
V_{FEH} 2/	FE supply (Program)	I_{FEH} = 300 ±25 mA (Transient or steady state)	16.0	17.0	18.0	V
V_{FEL}	FE supply (Idle)		1.25	1.5	1.75	V

See footnotes at end of table.

TABLE IV. Programming characteristics - Circuit A 4/ - Continued.

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Type	Max	
I_{FEH}	FE supply current limit	V_{FEH} = +17 ±1.0 V	275	300	325	mA
V_{CCP} 1/	V_{CC} supply (Program "AND")	I_{CCP} = 550 mA, min (Transient or steady state)	4.75	5.0	5.25	V
I_{CCP}	I_{CC} limit (Program "AND")	V_{CCP} = +5.0 ±.25 V	550		1,000	mA
V_{OPF}	Forced output (Program)		9.5	10	10.5	V
I_{OPF}	Output current (Program)				10	mA
T_R	Output pulse rise time		10		50	µs
t_P	CE programming pulse width		1		1.5	ms
t_D	Pulse sequence delay		10			µs
T_{PR}	Programming time			.6		ms
$\frac{T_{PR}}{T_{PR} + T_{PS}}$	Programming duty cycle				50	%
F_L	Fusing attempts per link				2	cycle
V_S 3/	Verify threshold		1.4	1.5	1.6	V

1/ Bypass V_{CC} to GND with a 0.01 µf capacitor to reduce voltage spikes.

2/ Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

3/ V_S is the sensing threshold of the FPLA output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

4/ These are specifications which a Programming System must satisfy.

5/ T_C = 25°C.

TABLE V. Programming specifications - Circuit B.

Symbol	Characteristic	Recommended 1/				Comments
		Min	Value	Max	Units	
V_{IH}	TTL levels	2.4	5.0	5.0	V	Apply to appropriate address and output pins. Do not leave pins open.
V_{IL}		0	0	0.4	V	
$\overline{CE}$	Chip select	2.4	5.0	5.0	V	
V_{OP}	Programming voltage pulse	17.5	18.0	18.5	V	Apply to the appropriate output pin.
t_{PW}	Programming pulse width		0.18	50	ms	
	Duty cycle, programming pulse		20		%	Maximum duty cycle to maintain T_C < 85°C
t_r	Programming pulse rise time	0.5	1.0	3.0	µs	
	Number of pulses required	1	4	8		
V_{CC}	Power supply voltage	4.9	5.0	5.1	V	
t_c	Case temperature		25	85	°C	
I_{VP}	Programming pulse current max (V_P pin)			200	mA	If pulse generator is used, set current limit to this max value.
I_{OP}	Programming pulse current max (any output pin)			100	mA	If pulse generator is used, set current limit to this max value.
V_{CC}	Low V_{CC} read		4.4	5.0	V	Programming read verify.
V_P	Programming voltage	14.5	15.0	15.5	V	Pin 1

1/ T_C = 25°C.

TABLE VI. Summary of pin voltages - Circuit B.

	Read	Program product "AND" matrix	Verify product "AND" matrix	Program summing matrix	Verify summing matrix	Program output polarity	Verify output polarity
Pin 1 (FE)	***	18	***	***	***	***	***
Pin 2 (I7)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 3 (I6)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 4 (I5)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 5 (I4)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 6 (I3)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 7 (I2)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 8 (I1)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 9 (I0)	TTL	12.0*	12.0*	TTL	TTL	TTL HIGH	TTL HIGH
Pin 10 (F7)	READ	TTL	TTL	****	READ	****	READ
Pin 11 (F6)	READ	TTL	TTL	****	READ	****	READ
Pin 12 (F5)	READ	TTL	TTL	****	READ	****	READ
Pin 13 (F4)	READ	TTL	TTL	****	READ	****	READ
Pin 14 (GND)	GND	GND	GND	GND	GND	GND	GND
Pin 15 (F3)	READ	TTL	TTL	****	READ	****	READ
Pin 16 (F2)	READ	TTL	TTL	****	READ	****	READ
Pin 17 (F1)	READ	**	**	****	READ	****	READ
Pin 18 (F0)	READ	READ	READ	****	READ	****	READ
Pin 19 ($\overline{CE}$)	TTL LOW	TTL HIGH	TTL HIGH	TTL HIGH	TTL LOW	TTL HIGH	TTL LOW
Pin 20 (I15)	TTL	12.0*	12.0*	TTL HIGH	TTL HIGH	TTL HIGH	12.0
Pin 21 (I14)	TTL	12.0*	12.0*	TTL HIGH	12.0	12.0	TTL HIGH

See footnotes at end of table.

TABLE VI. Summary of pin voltages - Circuit B - Continued.

	Read	Program product "AND" matrix	Verify product "AND" matrix	Program summing matrix	Verify summing matrix	Program output polarity	Verify output polarity
Pin 22 (I13)	TTL	12.0*	12.0*	12.0	TTL HIGH	12.0	TTL HIGH
Pin 23 (I12)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 24 (I11)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 25 (I10)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 26 (I9)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 27 (I8)	TTL	12.0*	12.0*	12.0	12.0	12.0	12.0
Pin 28 (V_{CC})	5.0	5.0	5.0	5.0	12.0	5.0	5.0

*For selection of input apply TTL HIGH or TTL LOW
**Left open or TTL HIGH.
***Left open or grounded.
****Left open, TTL HIGH, or programming pulse.
The program table is used for coding FPLAs.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883). Test condition D or E using the burn-in circuit as shown on figure 4 or equivalent.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) for class S devices shall be as specified in MIL-M-38510. The PDA for class B devices shall be 10 percent based on failures from group A, subgroups 1 and 7 test after cooldown of final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot. The lot shall be accepted or rejected based on the PDA for the applicable device class.

d. Freeze-out test. This test shall be conducted as a 100 percent screen on all class S devices and as an additional subgroup for group C for class B and class C devices (see 4.4.2d). Within no more than 24 hours after completion of burn-in and prior to final electrical test, all devices containing nichrome resistors (see 3.7.1 and 3.7.2) shall be subjected to a freeze-out test. If more than 24 hours have elasped subsequent to the 125°C burn-in exposure, devices shall be conditioned with at least 125°C for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is performed, the 25°C final electrical test parameters shall be completed 96 hours after completion of the freeze-out test. The freeze-out test shall be conducted as follows:

1. Connect devices in the electrical configuration of figure 7 or in the burn-in configuration of figure 4 with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of the test.

2. Reduce device temperature to T_A = -10° ±2°C with the bias cycled and maintain at that temperature for a minimum of 5 hours duration.

3. With the cycled bias maintained, allow T_A to go to room temperature (by removal from the cold chamber or termination of forced cooling but with no forced heating) and retain for a minimum of 19 hours subsequent to the completion of the 5-hour cold soak. T_A shall not exceed 35°C during this period.

4. Remove bias and subject all devices to subgroup 1 final electrical test to establish continuity of the nichrome resistors and remove all failed devices from the lot. For class S devices count them as screening rejects subject to the PDA requirements of 4.2c.

e. All devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7, 8, 9, 10, and 11 shall be by attributes only.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II.

b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve (12) devices shall be submitted to programming (see 3.2.2.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturers option, the sample may be increased to 24 total devices with no more than four total device failures allowable.

d. For unprogrammed devices, ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail in all three subgroups, the lot shall be rejected. At the manufacturers option, the sample may be increased to twenty total devices with no more than four total device failures allowable.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

a. Water drop test. This test shall be added to group B for class S devices. The devices selected for subgroup 2(b) testing shall be a sealed, electrically good unprogrammed device which has passed the applicable screening and group A electrical test requirements. The device shall be carefully delidded and functionally verified to contain no programmed bits. Power shall be applied (or continuously cycled through its test sequence), for the duration of the test. A drop of deionized water (resistivity of 5 megohms minimum at the point of use and at 25°C) shall be placed on the memory element containing nichrome film resistors so as to completely cover a minimum of 25 percent of the memory bits without touching any bonding pads, wires, or exposed metallization. Examination of the water drop at 20X magnification during placement with a micropipette is sufficient to determine coverage. The water drop shall be allowed to remain with the device under power for a minimum of 3 minutes duration. The power shall be removed, the device dried, and the device functionally verified to contain no programmed bit. Failure of any functional test which results from an open thin nichrome resistor (other than test equipment induced) shall fail the lot.

b. Class S devices selected for testing in subgroup 5 (table IIa of method 5005 of MIL-STD-883) shall be programmed in accordance with 3.2.2.

c. Steady state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883 using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 5 or equivalent shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady state life test (method 1005 of MIL-STD-883) conditions:

1. Test condition D or E, using the circuit shown on figure 4, or equivalent.

2. T_A = 125°C minimum.

3. Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

c. For qualification, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.2.2). For Quality Conformance Inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.

d. For classes B and C devices, the freeze-out test shall be added to group C as subgroup 3 (see 4.2d) and shall be conducted with an LTPD = 10. Perform steps 1, 2, and 3 of 4.2d three times for a total test duration of 72 hours before performing step 4.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883; end-point electrical parameters shall be as specified in table II herein.

4.4.5 Inspection of packaging. The sampling and inspection of the preservation-packaging, packing, and container marking shall be in accordance with the requirements of MIL-M-38510, except that the rough-handling test shall not apply.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure for circuit A. The programming specifications in table IV and the following procedures shall be used for programming the device.

4.6.1 Output polarity.

4.6.1.1 Program active low (F_p function). Program output polarity before programming "AND" matrix and "OR" matrix. Program 1 output at a time. (S) links of unused outputs are not required to be fused.

a. Set GND (pin 14), and FE (pin 1) to 0 V.

b. Set V_{CC} (pin 28) to V_{CCL}.

c. Set $\overline{CE}$ (pin 19), and I_0 through I_{15} to V_{IH}.

d. Apply V_{OPH} to the appropriate output, and remove after a period t_p.

e. Repeat step D to program other outputs.

4.6.1.2 Verify output polarity.

a. Set GND (pin 14) to 0 V, and V_{CC} (pin 28) to V_{CCS}.

b. Enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.

c. Address a non-existent P-term by applying V_{IH} to all inputs I_0 through I_{15}.

d. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a high logic level are programmed active low (F_p function), while all outputs at a low logic level are programmed active high (F_p function).

e. Return V_{CC} to V_{CCP} or V_{CCL}.

f. For class S and B devices, if any output polarity does not verify as programmed, it shall be considered a programming reject. For class C devices, if any output does not verify as programmed, repeat 4.6.1.1 one time only. Outputs which fail to program the second time shall be considered programming rejects.

4.6.2 "AND" Matrix.

4.6.2.1 Programming input variable. Program 1 input at a time and 1 P-term at a time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

a. Set GND (pin 14) to 0 V, and V_{CC} (pin 28) to V_{CCP}.

b. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.

c. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

d. Address the P-term to be programmed (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels V_{OHF} and V_{OLF}.

e. If the P-term contains neither I_0 or $\overline{I}_0$ (input is a Don't Care), fuse both I_0 and $\overline{I}_0$ links by executing both steps f and g, before continuing with step k.

f. If the P-term contains I_0, set to fuse the $\overline{I}_0$ link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute steps h, i, and j.

g. If the P-term contains $\overline{I}_0$, set to fuse the I_0 link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute steps h, i, and j.

h. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

i. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.

j. After t_D delay, return FE input to V_{FEL}.

k. Disable programmed input by returning I_0 to V_{IX}.

l. Repeat steps e through k for all other input variables.

m. Repeat steps d through e for all other P-terms.

n. Remove V_{IX} from all input variables.

4.6.2..2 Verify input variable.

a. Set GND (pin 14) to 0 V, V_{CC} (pin 28) to V_{CCP}, and FE (pin 1) to V_{FEL}.

b. Enable F_7 output by setting CE to V_{IX}.

c. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

d. Address the P-term to be verified (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5.

e. Interrogate input variable I_0 as follow:

1. Lower the input voltage to I_0 from V_{IX} to V_{IH}, and sense the logic state of output F_7.

2. Lower the input voltage to I_0 from V_{IH} to V_{IL}, and sense the logic state of output F_7.

f. The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	Input variable state contained in P-term 1/
0 1	1 0	$\overline{\overline{I_0}}$
0 1	0 1	I_0
0 1	1 1	Don't care
0 1	0 0	(I_0), $(\overline{I_0})$

1/ Two tests are required to uniquely determine the state of the input variable contained in the P-term.

g. Disable verified input by returning to I_0 to V_{IX}.

h. Repeat steps e and g for all other input variables.

i. Repeat steps d through h for all other P-terms.

j. Remove V_{IX} from all input variables.

k. For class S and B devices, if any gate does not verify as programmed, it shall be considered a programming reject. For class C devices, if any gate does not verify as programmed, repeat 4.6.2.1 one time only. Gates which fail to program the second time shall be considered programming rejects.

4.6.3 "OR" (Sum) Matrix.

4.6.3.1 Program product term. Program 1 output at a time for a P-term at the time. All P_n links in the "OR" matrix corresponding to unused outputs and unused P-terms are not required to be fused.

a. Set GND (pin 14) to 0 V, and V_{CC} (pin 28)to V_{CCS}.

b. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.

c. Set inputs I_6 through I_{15} to V_{IH} or V_{IL}.

d. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB.

e. If the P-term is contained in output function F_0 (F_0 = 1 or F_0 = 0), go to step g, (fusing cycle not required).

f. If the P-term is not contained in output function F_0 (F_0 = 0 or F_0 = 1), set to fuse the P_n link by forcing output F_0 to V_{OPF}.

g. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

h. After t_D delay, pulse the CE input from V_{IH} to V_{IX} for a period t_p.

i. After t_D delay, return FE input to V_{FEL}.

j. After t_D delay, remove V_{OPF} from output F_O.

k. Repeat steps e through j for all other output functions.

l. Repeat steps d through k for all other P-terms.

m. Remove V_{CCS} from V_{CC}.

4.6.3.2 Verify product term.

a. Set GND (pin 14) to 0 V, and V_{CC} (pin 28) to V_{CCS}).

b. Enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.

c. Set inputs I_0 through I_{15} to V_{IH} and V_{IL}.

d. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5.

e. To determine the status of the P_n link in the "OR" matrix for each output function F_p or F_p sense, the state of outputs F_0 through F_7. The status of the link is given by the following truth table.

Output		P-term link
Active high (F_p)	Active low ($F_p^{\bullet}$)	
0	1	Fused
1	0	Present

f. Repeat steps d and e for all other P-terms.

g. Remove V_{CCS} from V_{CC}.

h. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.6.3.1, one time only. Bits which fail to program the second time shall be considered programming rejects.

4.7 Programming procedure for circuit B. The programmed specifications on table V and the following procedures shall be used for programming the device.

4.7.1 Program "PRODUCT (AND)" matrix.

4.7.1.1 All 48 AND gates of the product matrix are fuse linked to both the true and false lines of every input buffer in the initial unprogrammed state. The initial logic expression for the 48 unprogrammed AND gates is $I_0 \bullet \overline{I_0} \bullet I_1 \bullet \overline{I_1} \bullet I_{15} \bullet \overline{I_{15}}$ (where In or $\overline{In}$ is defined to be an input term). Programming the fuse located by the selection of an input line, 'i_n', and the mth AND gate replaces the input term In with '1' in the logic expression for the mth AND gate.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL HIGH level.

d. Apply TTL levels to pins 10 through 13, 15, and 16 (F_7 through F_2) to address an on-chip one of forty-eight decoder to select the AND gate to be programmed (F_7 = LSB and F_2 = MSB).

e. Apply 12.0 V to all input pins (I_0 through I_{15}).

f. Apply the proper TTL level to an Ix input pin as follows (program one input at a time):

1. If the product term to be programmed contains the input term Ix (where x = 0 through 15), lower the Ix pin to a TTL HIGH level.

2. If the product term to be programmed contains the input term Ix, lower the $\overline{Ix}$ to a TTL LOW level.

3. If the product term does not contain the input terms $\overline{Ix}$ or Ix (i.e., Ix is a DON'T CARE input), perform steps F1, G, F2, and G.

g. Apply a 15 V programming pulse to pin 1 (FE) according to the programming specifications table.

h. Repeat steps e through g for each input of the selected product term.

i. Repeat steps d through h for all other product terms to be programmed.

j. Program one input at a time.

k. All unused inputs of programmed product terms must be programmed as DON'T CARES.

l. Inputs of unused product lines are not required to be programmed.

m. Pin 18 (F_0) is in the read mode (open collector). Care must be taken so that this pin is either left open, grounded, or loaded such that the current flowing into the pin does not exceed 16 mA.

4.7.1.2 Verify "PRODUCT (AND)" matrix.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL HIGH level.

d. Apply TTL levels to pins 10 through 13, 15, and 16 (F_7 through F_2) to address an on-chip one of forty-eight decoder to select the AND gate to be verified (F_7 = LSB and F_2 = MSB).

e. Apply 10.8 V to all input pins (I_0 through I_{15}).

f. Test the state of the Ix input as follows:

1. Lower the Ix pin to a TTL HIGH level and sense the voltage on pin 18 (F_0).

2. Lower the Ix pin to a TTL LOW and sense the voltage on pin 18 (F_0).

g. The state of the Ix input is determined as follows:

	Ix = TTL HIGH	Ix = TTL LOW	Condition of Ix for selected product term
Level at output F_0	H	H	Don't care
	H	L	Ix IN P-term
	L	H	Ix IN P-term
	L	L	Unprogrammed

NOTES:
1. F_0 in this mode functions as an open collector output, H = $\geq$ 2.0 V, L $\leq$ 0.8 V.
2. The table above is valid regardless of the polarity (active HIGH or active LOW) of F_0.
3. Pin 1 (FE) should be either floating or grounded.

4.7.2 Program summing matrix.

4.7.2.1 All 8 OR gates of the summing matrix are fuse linked to the outputs of the AND gates in the initial unprogrammed state. The initial logic expression (sum of products) of the 8 unprogrammed OR gates is P0 + P1 + P2 + ••• +P47 where Pm is the product term programmed into the mth AND gate. Programming the fuse located by the selection of the mth AND gate and the nth summing line replaces the product term Pm with '0' in the logic expression of the nth OR gate. The nth summing line is selected by the selection of the nth output buffer where n = 1 though 8.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL HIGH level.

d. Apply TTL levels to pins 4 through 9 (I_5 through I_0) to address an on-chip one of forty-eight decoder to select the AND gate to be programmed (I_0 = LSB and I_5 = MSB).

e. Apply a TTL HIGH level to pins 20 and 21 (I_{15} and I_{14}).

f. Connect the remaining input pins to 12.0 V.

g. Apply an 18 V programming pulse (see programming specifications table) at the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

h. Program one output pin at a time.

i. All unused product lines are not required to be programmed.

4.7.2.2 Verify summing matrix.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL LOW level.

d. Apply TTL levels to pins 4 through 9 (I_5 through I_0) to address an on-chip one of forty-eight decoder to select the AND gate to be verified (I_0 = LSB and I_5 = MSB).

e. Apply A TTL HIGH level to pins 20 and 22 (I_{15} and I_{13}).

f. Connect the remaining input pins to 12.0 V

g. Sense the voltage on the output pin to be verified. The programming of the selected product line to the output line can be determined as follows:

Output reads	Fuse link
L	Blown (inactive
H	Unblown (active

h. Repeat steps d through g with V_{CC} at 4.4 V (LOW V_{CC} read).

i. The condition of the fuse link can be determined from the table above regardless of the polarity (active HIGH or active LOW) of the output buffer being verified.

4.7.3 Program output polarity.

4.7.3.1 The initial unprogrammed state of all eight output buffers is active LOW or iverting. To program an output buffer into the active HIGH or non-inverting state, proceed as follows:

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL HIGH level.

d. Apply a TTL HIGH level to pins 4 through 9 (I_5 through I_0).

e. Apply a TTL HIGH level to pin 20 (I_{15}).

f. Connect the remaining input pins to 12.0 V.

g. Apply an 18 V programming pulse (see programming specifications table) to the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

h. Program one output at a time.

4.7.3.2 Verify output polarity.

a. Connect pin 28 (V_{CC}) to 5.0 V.

b. Connect pin 14 (GND) to ground.

c. Connect pin 19 ($\overline{CE}$) to a TTL LOW level.

d. Apply a TTL HIGH level to pins 4 through 9 (I_5 through I_0).

e. Apply a TTL HIGH level to pins 21 and 22 (I_{14} and I_{13}).

f. Connect the remaining input pins to 12.0 V.

g. Sense the voltage on the pin of the output buffer to be verified. The condition of the output can be determined as follows:

Output reads	Output state
H	Active LOW
L	Active HIGH

h. Repeat with V_{CC} at 4.4 V (LOW V_{CC} read).

4.7.4 Summary of pin voltages - circuit B. In addition to verifying the Product (AND) Matrix, Summing Matrix, and Output Polarity separately after programming, a complete logic verification (normal read) with V_{CC} at 5.0 V is recommended after a device has been fully programmed. Table VI summarizes the full programming and verifying procedures.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

h. Requirement for programming the device, including processing option.

i. Requirement for "JAN" marking.

j. Requirements for packaging and packing.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	Electrical ground (common terminal).
V_{IN}	Voltage level at an input terminal.
V_{IC}	Input clamp voltage.
I_{IN}	Current flowing into an input terminal.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be procured in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification shall functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	Circuit A, Signetics Corp 82S101
01	Circuit B, Fairchild 93458
02	Circuit A, Signetics Corp 82S100
02	Circuit B, Fairchild 93459

Custodian:
Air Force - 17

Review activities:
Air Force - 11, 19, 85, 99
DLA - ES

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-F483)

APPENDIX

GATE TEST PROGRAM AND FUNCTIONAL TESTS

10. SCOPE

10.1 This appendix covers the fuse test program to be used for unprogrammed devices, and defines the requirements for functional tests of unprogrammed devices.

20. Gate test program.

20.1 When required, as in paragraph 3.2.2.1, the device may be programmed as shown in table VII. This program will allow for testing all of the available gates.

30. Fuse tests for device types 01 and 02.

30.1 Unprogrammed devices - Circuit A.

30.1.1 Output polarity fuse check.

Terminal conditons:

V_{CC} = 8.5 V
FE = 1.5 V
CE = GND
All inputs = 3.0 V

a. Sense all outputs for logic low, any high is a failure.

30.1.2 "AND" matrix fuse check.

Terminal conditons:

V_{CC} = 4.5 V
FE = 1.5 V
CE = 10 V
All inputs = 10 V (except for input being checked)

a. Address all "P" terms with a binary count 0-47, put into F_0 to F_5 with F_0 = LSB and F_5 = MSB.

b. Sense output F_7 for each "P" term. F_7 should also be low and if it goes high, then it means a failure since a fuse is open. The input being checked should be set first to V_{IH} and then V_{IL}. F_7 should remain low in both cases.

c. Repeat b for all inputs, one at a time.

d. Repeat a and then b for all "P" terms and their inputs.

30.1.3 "OR" (Sum) matrix fuse check.

Terminal conditons:

V_{CC} = 8.5 V
FE = 1.5 V
I_6 - I_{15} = Open
I_0 - I_5 = Binary Count Input for address
$\overline{CE}$ = GND

a. Sense each output for logic high. Any low is a failure, indicating a fuse open.

b. Sense all output low when binary input count goes to 48. Any high is a failure.

30.2 Unprogrammed devices - Circuit B.

30.2.1 "AND" (Product) matrix input fuse check.

Terminal conditons: V_{CC} = 5.0 V
$\overline{CE}$ = TTL HIGH

a. Select the product term to be tested by applying a binary address of TTL levels to pins 10 thru 13, 15, 16 (F_7 thru F_2) (F_7 = LSB, F_2 = MSB).

b. Apply 12.0 V to all input pins (I_0 thru I_{15}) except for input Ix being tested.

c. The state of the Ix input fuse will be checked if the truth table below holds. Vary input Ix while monitoring pin 18 (F_0),

Ix	F_0
L	L
H	L

If F_0 is HIGH, then fuse is open indicating a failure.

d. Repeat steps b and c for each input of the selected product term.

e. Repeat steps a thru c for all other product items and input fuse tests.

30.2.2 "OR" (Sum) matrix fuse check.

Terminal conditons: V_{CC} = 5.0 V
$\overline{CE}$ = TTL LOW

a. Apply TTL levels to pins 4 thru 9 (I_5 thru I_0) to select the AND gate to be verified (I_0 = LSB and, I_5 = MSB).

b. Apply TTL HIGH level to pins 20 and 22 (I_{15} and I_{13}).

c. Connect the remaining input pins to 12.0 V.

d. Sense the voltage on the output pin to be verified. All unblown fuse links will indicate a high on the output pin.

30.2.3 Output polarity fuse check.

Terminal conditons: V_{CC} = 5.0 V
$\overline{CE}$ = TTL LOW

a. Apply TTL HIGH level to pins 4 thru 9 (I_5 thru I_0), 21 and 22 (I_{14} and I_{13}).

b. Connect remaining pins to 12.0 V.

c. Sense the voltage on the pins of the output buffer to be verified. All output levels should read TTL HIGH.

30.3 Programmed devices - Circuits A and B.

Program the device according to the program shown in table VII.

TABLE VII. Program tables for test device.

Program table entries						
Input variable			Output function		Output active level	
I_m	$\overline{I}_m$	Don't care	Prod. term present in Fp	Prod. term Not present in Fp	Active High	Active Low
H	L	- (dash)	A	.(period)	H	L
NOTE: Enter (-) for unused inputs of used P-terms			NOTES: 1. Entries independent of output polarity. 2. Enter (A) for unused outputs of used P-terms.		NOTES: 1. Polarity programmed once only. 2. Enter (H) for all unused outputs.	

Product term*																Active level							
	Input variable															L	L	L	L	H	H	H	H
No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Output function*							
																	7	6	5	4	3	2	1	0
0	-	-	-	-	-	-	L	-	H	-	-	-	-	-	-	H	.	.	.	A	.	.	.	A
1	-	-	-	-	-	-	L	L	H	-	-	-	H	-	-	-	.	.	.	A	.	.	.	A
2	-	-	-	-	-	-	L	-	H	-	-	-	-	-	H	-	.	.	A	.	.	.	A	.
3	-	-	-	-	-	-	L	L	H	-	-	H	-	-	-	-	.	.	A	.	.	.	A	.
4	-	-	-	-	-	-	L	-	H	-	-	-	-	H	-	-	.	A	.	.	.	A	.	.
5	-	-	-	-	-	-	L	L	H	-	H	-	-	-	-	-	.	A	.	.	.	A	.	.
6	-	-	-	-	-	-	L	-	H	-	-	-	H	-	-	-	A	.	.	.	A	.	.	.
7	-	-	-	-	-	-	L	L	H	H	-	-	-	-	-	-	A	.	.	.	A	.	.	.
8	-	-	-	-	-	-	L	L	L	-	-	-	H	-	-	H	.	.	.	A	.	.	.	A
9	-	-	-	-	-	-	L	L	L	-	-	H	-	-	H	-	.	.	A	.	.	.	A	.
10	-	-	-	-	-	-	L	L	L	-	H	-	-	-	H	-	.	A	.	.	.	A	.	.
11	-	-	-	-	-	-	L	L	L	H	-	-	-	H	-	-	A	.	.	.	A	.	.	.
12	-	-	-	-	-	-	H	H	H	-	-	-	H	-	-	-	.	.	.	A	.	.	.	A
13	-	-	-	-	-	-	H	H	H	-	-	H	-	-	-	-	.	.	A	.	.	.	A	.
14	-	-	-	-	-	-	H	H	H	-	H	-	-	-	-	-	.	A	.	.	.	A	.	.
15	-	-	-	-	-	-	H	H	H	H	-	-	-	-	-	-	A	.	.	.	A	.	.	.
16	-	-	-	-	L		H	L	L	-	-	-	L	-	-	-	.	.	.	A	.	.	.	A
17	-	-	-	-	L		H	L	L	-	-	-	H	-	-	L	.	.	.	.	.	.	.	A
18	-	-	-	-	H		H	L	L	-	-	-	L	-	-	L	.	.	.	.	.	.	.	A
19	-	-	-	-	H		H	L	L	-	-	-	H	-	-	H	.	.	.	.	.	.	.	A
20	-	-	-	H	-		H	L	L	-	-	L	-	-	H	-	.	.	.	.	.	.	A	.
21	-	-	-	H	-		H	L	L	-	-	H	-	-	L	-	.	.	.	.	.	.	A	.
22	-	-	-	L	-		H	L	L	-	-	L	-	-	L	-	.	.	.	.	.	.	A	.
23	-	-	-	L	-		H	L	L	-	-	H	-	-	H	-	.	.	.	.	.	.	A	.
24	-	-	H	-	-		H	L	L	-	L	-	-	-	H	-	.	.	.	.	.	A	.	.
25	-	-	H	-	-		H	L	L	-	H	-	-	-	L	-	.	.	.	.	.	A	.	.
26	-	-	L	-	-		H	L	L	-	L	-	-	-	L	-	.	.	.	.	.	A	.	.
27	-	-	L	-	-		H	L	L	-	H	-	-	-	H	-	.	.	.	.	.	A	.	.
28	-	H	-	-	-		H	L	L	L	-	-	-	H	-	-	.	.	.	.	A	.	.	.
29	-	H	-	-	-		H	L	L	H	-	-	-	L	-	-	.	.	.	.	A	.	.	.
30	-	L	-	-	-		H	L	L	L	-	-	-	L	-	-	.	.	.	.	A	.	.	.
31	-	L	-	-	-		H	L	L	H	-	-	-	H	-	-	.	.	.	.	A	.	.	.
32	-	L	-	-	-		H	L	L	-	-	-	-	H	-	-	.	.	.	A	.	.	.	.
33	-	L	-	-	-		H	L	L	H	-	-	-	-	-	-	.	.	.	A	.	.	.	.
34	-	-	-	-	H		H	L	L	-	-	-	-	-	-	H	.	.	A	.	.	.	.	.
35	-	-	-	-	H		H	L	L	-	-	-	H	-	-	-	.	.	A	.	.	.	.	.
36	-	-	-	L	-		H	L	L	-	-	-	-	-	-	H	.	A	.	.	.	.	.	.
37	-	-	-	L	-		H	L	L	-	-	H	-	-	-	-	.	A	.	.	.	.	.	.
38	-	-	L	-	-		H	L	L	-	-	-	-	-	H	-	A	.	.	.	.	.	.	.
39	-	-	L	-	-		H	L	L	-	H	-	-	-	-	-	A	.	.	.	.	.	.	.
40	-	-	-	-	-		H	L	L	H	-	-	-	H	-	-	.	.	.	A	.	.	.	.
41	-	-	-	-	-		H	L	L	-	-	-	H	-	-	H	.	.	A	.	.	.	.	.
42	-	-	-	-	-		H	L	L	-	-	H	-	-	-	H	.	A	.	.	.	.	.	.
43	-	-	-	-	-		H	L	L	-	H	-	-	-	H	-	A	.	.	.	.	.	.	.
44	H	H	H	H	H		H	H	H	H	H	H	H	H	H	H	A	A	A	A	A	A	A	A
45	L	L	L	L	L		L	L	L	L	L	L	L	L	L	L	A	A	A	A	A	A	A	A
46	L	L	L	L	L		L	L	L	H	H	H	H	H	H	H	A	A	A	A	A	A	A	A
47	H	H	H	H	H		H	H	H	L	L	L	L	L	L	L	A	A	A	A	A	A	A	A

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